Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A process for transmitting at given instants digital signals on a bus, said digital signals being transmitted on the bus selectively in a non-encoded format and in an encoded format so as to minimize a switching activity on the bus, the process comprising:

associating to said digital signals an additional signal that is able to assume, at said given instants, different logic values according to whether the digital signal to which it is associated is transmitted in said non-encoded format and, at least in part, in said encoded format, respectively, so that said additional signal is able to modify its logic value between successive instants of said given instants;

detecting for said digital signals a condition in which transmission on said bus in said non-encoded format and in said encoded format are able to give rise to an identical switching activity on the bus; and

determining whether a digital signal to be transmitted on the bus at a given instant is to be transmitted in said non-encoded format or in said at least partially encoded format so as to cause the additional signal associated to said signal to be transmitted on the bus at a given instant to keep a logic value with respect to a logic value assumed by the additional signal for transmission on the bus for a preceding instant among said given instants.

2. (Original) The process according to claim 1, wherein:

determining whether to transmit a signal on the bus in non-encoded format or in encoded format comprises comparing the signal to be transmitted on the bus for an instant of said given instants with a signal transmitted on the bus for a preceding instant among said given instants

bit by bit in orderly sequence so as to identify a first set of bits that are not changed and a second set of bits at least some of which are changed; and

determining whether to transmit said signal on the bus in non-encoded format and in encoded format limitedly to bits of said second set of bits.

3. (Original) The process according to claim 2, further comprising identifying, in the context of said orderly sequence, at least one marker bit that separates bits of said first set from bits of said second set.

4. (Original) The process according to claim 2 wherein the comparison bit by bit is carried out starting from a bit with a least probability of change.

5. (Original) The process according to claim 2 wherein the comparison bit by bit is carried out starting from a most significant bit.

6. (Original) The process according to claim 2 wherein the comparison bit by bit is carried out starting from a least significant bit.

7. (Original) The process according to claim 2 wherein the comparison bit by bit is carried out starting from a given bit, exploring other bits subjected to comparison moving in a given direction.

8. (Original) The process according to claim 2 wherein the comparison bit by bit is carried out starting from at least one given bit, exploring other bits subjected to comparison moving in opposite directions.

9. (Original) The process according to claim 1, further comprising transmitting, in non-encoded format, a first bit of said signal to be transmitted on the bus.

10. (Original) The process according to claim 2, further comprising encoding integrally, in view of transmission on the bus, said signal to be transmitted on the bus if said comparison operation reveals that a first bit considered in said orderly sequence is changed.

11. (Original) The process according to claim 2 wherein the first set of bits are transmitted in non-encoded format.

12. (Currently Amended) The process according to claim 1, further comprising subjecting to logic inversion the bits of the signal in non-encoded format-.

13. (Original) The process according to claim 1, further comprising determining a distance between said signal to be transmitted on the bus at an instant among said given instants and the signal transmitted on the bus for the preceding instant among said given instants.

14. (Original) The process according to claim 13 wherein said distance is determined as Hamming distance.

15. (Original) An encoder for transmitting at given instants on a bus digital signals selectively in a non-encoded format and an encoded format, the encoder comprising:

a transmission-driving module for driving transmission of said signals on the bus in non-encoded format and in encoded format so as to minimize a switching activity on the bus; and

a module for associating to said digital signals an additional signal that is able to assume, at said given instants, different logic values according to whether the digital signal to which it is associated is transmitted in said non-encoded format or, at least in part, in said encoded format, respectively, so that said additional signal is able to modify its logic value between successive instants of said given instants; and

a module for detecting, for said digital signals a condition in which the transmission on said bus in said non-encoded format and in said encoded format are able to give rise to an identical switching activity on the bus, wherein

said transmission-driving module is configured to drive transmission of said signals on the bus in said non-encoded format and in said at least in part encoded format so as to cause the additional signal associated to said signal to be transmitted on the bus at a given instant to keep its logic value with respect to a logic value assumed by the additional signal for transmission on the bus for a preceding instant among said given instants.

16. (Currently Amended) The encoder according to claim 15, further comprising:

a comparison module for comparing a signal to be transmitted on the bus for an instant of said given instants with a signal transmitted on the bus for a preceding instant among said given instants, and emitting at least one corresponding decision signal; said comparison module comprising a logic network that is able to compare bit by bit, in orderly sequence, said signal to be transmitted on the bus at an instant of said given instants and said signal transmitted on the bus for the preceding instant among said given instants, so as to identify a first set of bits that are not changed and a second set of bits at least some of which are changed; and,

said transmission-driving module ~~(14, 15)~~ is configured for driving the transmission of said signals on the bus in non-encoded format and in encoded format limitedly to the bits of said second set of bits.

17. (Original) The encoder according to claim 16 wherein said logic network compares bit by bit, starting from a bit with a least probability of change.

18. (Original) The encoder according to claim 16 wherein said logic network compares bit by bit, starting from a most significant bit.

19. (Original) The encoder according to claim 16 wherein said logic network compares bit by bit, starting from a least significant bit.

20. (Original) The encoder according to claim 16 wherein said logic network compares bit by bit starting from a given bit, exploring other bits subjected to comparison, moving in a given direction.

21. (Original) The encoder according to claim 16 wherein said logic network compares bit by bit starting from at least one given bit, exploring other bits subjected to comparison, moving in opposite directions.

22. (Original) The encoder according to claim 15 wherein said transmission-driving module is configured to drive transmission of a first bit of said signal to be transmitted on the bus in non-encoded format.

23. (Original) The encoder according to claim 16 wherein said transmission-driving module is configured to drive transmission of said signal to be transmitted on the bus in integrally encoded format, if said logic network indicates that a first bit considered in said orderly sequence is changed.

24. (Original) The encoder according to claim 16 wherein said transmission-driving module is configured for transmitting on the bus said first set of bits always in non-encoded format.

25. (Currently Amended) The encoder according to claim 15, further comprising an inverter circuit for generating said encoded format_subjecting to logic inversion the bits of the signal in non-encoded format.

26. (Original) The encoder according to claim 15, further comprising a module for calculating a distance for determining said switching activity on the bus as distance between a signal to be transmitted on the bus at an instant among said given instants and a signal transmitted on the bus for a preceding instant among said given instants.

27. (Original) The encoder according to claim 26 wherein said at least one module for calculating distance comprises at least one module for calculating a Hamming distance.

28. (Currently Amended) A decoder for receiving digital signals transmitted on a bus-, comprising:

a decoding logic to identify for each digital signal received, at least one marker bit that separates a first set of bits in a non-encoded format from a second set of bits in an encoded format; and

a logic reconstruction network for reconverting from said encoded format to said non-encoded format the bits of said second set.

29. (Original) The decoder according to claim 28 wherein said decoding logic is able to identify said at least one marker bit as a bit of a digital signal with a least probability of change.

30. (Original) The decoder according to claim 28 wherein said decoding logic is able to identify said at least one marker bit as a most significant bit of a digital signal.

31. (Original) The decoder according to claim 28 wherein said decoding logic is able to identify said at least one marker bit as a least significant bit of a digital signal.

32. (Original) The decoder according to claim 28 wherein said decoding logic is able to identify said at least one marker bit as a starting bit for exploring a digital signal, carried out moving in a given direction.

33. (Original) The decoder according to claim 28 wherein said decoding logic is able to identify said at least one marker bit as a starting bit for exploring a digital signal, carried out moving in opposite directions.

34. (Original) The decoder according to claim 28 wherein the decoder is configured to assume as transmitted in non-encoded format a first bit of a digital signal.

35. (Original) The decoder according to Claim 28 wherein the decoder is configured to assume a larger set of the first and second set of bits is transmitted in said non-encoded format.

36. (Original) The decoder according to claim 28 wherein said logic reconstruction network reconverts said digital signals from said encoded format to said non-encoded format by means of logic inversion of bits subjected to encoding.

37. (Original) A computer program product directly loadable into the memory of a computer and comprising software code portions for:

associating with a digital signal an additional signal that is able to assume, at given instants, different logic values according to whether the digital signal to which it is associated is transmitted in a non-encoded format and, at least in part, in an encoded format, respectively, so that said additional signal is able to modify its logic value between successive instants of said given instants;

detecting for said digital signal a condition in which transmission on said bus in said non-encoded format and in said encoded format are able to give rise to an identical switching activity on the bus; and

determining whether a digital signal to be transmitted on the bus at a given instant is to be transmitted in said non-encoded format or in said at least partially encoded format so as to cause the additional signal associated to said signal to be transmitted on the bus at a given instant to keep a logic value with respect to a logic value assumed by the additional signal for transmission on the bus for a preceding instant among said given instants.

38. (Original) A computer program product which is directly loadable in the memory of a computer and comprising software code portions for driving transmission of signals on a bus in non-encoded format and in encoded format so as to minimize a switching activity on the bus by:

associating to said digital signals an additional signal that is able to assume, at given instants, different logic values according to whether the digital signal to which it is associated is transmitted in said non-encoded format or, at least in part, in said encoded format, respectively, so that said additional signal is able to modify its logic value between successive instants of said given instants; and

detecting for said digital signals a condition in which the transmission on said bus in said non-encoded format and in said encoded format are able to give rise to an identical switching activity on the bus, wherein transmission of said signals on the bus in said non-encoded format and in said at least in part encoded format is driven so as to cause the additional signal associated to said signal to be transmitted on the bus at a given instant to keep its logic value with respect to a logic value assumed by the additional signal for transmission on the bus for a preceding instant among said given instants.

39. (Original) A computer program product which is directly loadable into the memory of a computer and comprising software code portions for identifying for a digital signal received at least one marker bit that separates a first set of bits from a second set of bits; and reconverting from an encoded format to a non-encoded format only the bits of said second set.

40. (Original) A method of transmitting a signal on a bus, comprising:

comparing a first signal activity value associated with transmitting a signal in a first format with a second signal activity value associated with transmitting the signal in a second format;

if the first signal activity value is greater than the second signal activity value, transmitting the signal in the second format;

if the first signal activity value is less than the second signal activity value, transmitting the signal in the first format; and

if the first signal activity value is equal to the second signal activity value, comparing a third signal activity value associated with transmitting the signal in a first format with a fourth signal activity value associated with transmitting the signal is a second format, and

if the third signal activity value is greater than the fourth signal activity value, transmitting the signal in the second format; and

if the third signal activity value is less than the fourth signal activity value, transmitting the signal in the first format.

41. (Original) The method of claim 40 wherein the second format is an encoded format.

42. (Original) The method of claim 40 wherein the third signal activity value is associated with transmitting a control signal indicating the signal is being transmitted in the first format.

43. (Original) A transmitter for transmitting a signal on a bus, comprising:

a receiving module for receiving a signal to be transmitted;

a formatting module coupled to the receiving module, for formatting the received signal;

a module for calculating switching activity coupled to the receiving module and to the formatting module, for calculating first and second switching activity values associated with

transmitting the received signal and third and fourth switching activity values associated with transmitting the formatted received signal;

a comparator coupled to the module for calculating switching activity for comparing the first and third switching activity values and the second and fourth switching activity values; and

a driver coupled to the comparator, the receiving module and the formatting module, for driving transmission of one of the received signal and the formatted received signal, based, at least in part, on the comparisons of the first and third switching activity values and the second and fourth switching activity values.